CLAIM LISTING

1. (Previously Presented) A communications bus connected between a source node and a destination node, the communications bus including:

(a) a number of alternate transmission paths extending between the source node and the destination node on a common substrate comprising a semiconductor chip;

(b) a source switching arrangement interposed between the source node and the alternate transmission paths, the source switching arrangement being operable to selectively connect the source node to a selected one of the alternate transmission paths and disconnect the source node from each other alternate transmission path; and

(c) a destination switching arrangement interposed between the destination node and the alternate transmission paths, the destination switching arrangement being operable to selectively connect the destination node to the selected one of the alternate transmission paths and disconnect the destination node from each other alternate transmission path.

2. (Original) The communications bus of Claim 1 wherein:

(a) the source switching arrangement includes multiple source switching devices, a different source switching device connected between the source node and each alternate transmission path; and

(b) the destination switching arrangement includes at least one destination switching device connected between the destination node and each alternate transmission path.

3. (Original) The communications bus of Claim 1 wherein:

(a) the different source switching devices include at least one multiplexer; and

(b) the at least one destination switching device comprises a multiplexer.

4. (Original) The communications bus of Claim 1 further including:

(a) a source switch control structure for controlling the operation of the source switching arrangement; and

(b) a destination switch control structure for controlling the operation of the destination switching arrangement.

5. (Previously Presented) The communications bus of Claim 4 wherein the source switch control structure and the destination switch control structure each includes a nonvolatile or volatile memory structure.

6. (Original) The communications bus of Claim 1 further including test circuitry connected to the source node and destination node for applying a test signal to each alternate transmission path and for monitoring the destination node to determine whether the respective test signal is properly received at the destination node.

7. (Original) The communications bus of Claim 1 wherein:

(a) a receive node and first direction control node are associated with the source node, and a send node and second direction control node are associated with the destination node;

(b) a send switching arrangement is interposed between the send node and each alternate transmission path;

(c) a receive switching arrangement is interposed between each alternate transmission path and the receive node;

(d) a first direction control switching arrangement is interposed between the first direction control node and a control input of a tri-state driver associated with the source node; and

(e) a second direction control switching arrangement is interposed between the second direction control node and a control input of a tri-state driver associated with the send node.

8. (Original) The communications bus of Claim 1 wherein:

(a) the communications bus is also connected between a number of additional source nodes and the same number of additional destination nodes;

(b) a number of additional alternate transmission paths extend between each additional source node and each additional destination node;

(c) the source switching arrangement is also interposed between each additional source node and the respective alternate transmission paths associated with that respective additional source node, the source switching arrangement also being operable to selectively connect each respective additional source node to a selected one of the additional alternate transmission paths associated with that source node and disconnect each respective additional source node from each other additional alternate transmission path associated with that additional source node; and

(c) the destination switching arrangement is also interposed between each additional destination node and the respective alternate transmission paths associated with that additional destination node, the destination switching arrangement also being operable to selectively connect each respective additional destination node to the selected one of the alternate transmission paths associated with that additional destination node and disconnect the respective additional destination node from each other additional alternate transmission path associated with that additional destination node.

9. (Original) The communications bus of Claim 8 wherein the source switching arrangement comprises a number of multiplexers.

10. (Original) The communications bus of Claim 9 wherein the source node and number of additional source nodes are arranged side-by-side and wherein at least one pair of adjacent source nodes in this side-by side arrangement share a common multiplexer included in the number of multiplexers.

11. (Original) The communications bus of Claim 8 wherein:

(a) the source switching arrangement includes a first switching subset connected to a first subset of the alternate transmission paths;

(b) the source switching arrangement further includes a second switching subset connected to a second subset of the alternate transmission paths; and

(c) the alternate transmission paths making up the second subset of alternate transmission paths are interleaved with the alternate transmission paths making up the first subset of alternate transmission paths.

12. (Original) The communications bus of Claim 8 wherein:

(a) the source node and each additional source node is associated with a respective receive node and first direction control node, and the destination node and each additional destination node are associated with a respective send node and second direction control node;

(b) a send switching arrangement is interposed between the send nodes and the alternate transmission paths;

(c) a receive switching arrangement is interposed between the alternate transmission paths and the receive nodes;

(d) a first direction control switching arrangement is interposed between the first direction control nodes and a control input of a number of tri-state drivers, each driver associated with a respective source node; and

(e) a second direction control switching arrangement is interposed between the second direction control nodes and a control input of a number of additional tri-state drivers, each additional tri-state driver associated with a respective send node.

13. (Previously Presented) A communications bus connected between a number of source nodes and an equal number of destination nodes, the communications bus including:

(a) a number of alternate transmission paths extending between each respective source node and a matched one of the destination nodes on a common substrate comprising a semiconductor chip, the matched destination node being matched to a respective one of the source nodes;

(b) a source switching arrangement, the source switching arrangement being interposed between each respective source node and the respective alternate transmission paths associated with that respective source node, the source switching arrangement also being operable to selectively connect each respective source node to a selected one of the alternate transmission paths associated with that source node and disconnect each respective source node from each other alternate transmission path associated with that source node; and

(c) a destination switching arrangement, the destination switching arrangement being interposed between each respective destination node and the respective alternate transmission paths associated with that respective destination node, the destination switching arrangement also being operable to selectively connect each respective destination node to the selected one of the alternate transmission paths associated with that destination node and disconnect the respective destination node from each other alternate transmission path associated with that destination node.

14. (Original) The communications bus of Claim 13 wherein the source switching arrangement comprises a number of multiplexers.

15. (Original) The communications bus of Claim 14 wherein the source nodes are arranged side-by-side and wherein at least one pair of adjacent source nodes in this side-by side arrangement share a common multiplexer included in the number of multiplexers.

16. (Original) The communications bus of Claim 13 wherein:

(a) the source switching arrangement includes a first switching subset connected to a first subset of the alternate transmission paths;

(b) the source switching arrangement further includes a second switching subset connected to a second subset of the alternate transmission paths; and

(c) the alternate transmission paths making up the second subset of alternate transmission paths are interleaved with the alternate transmission paths making up the first subset of alternate transmission paths.

17. (Original) The communications bus of Claim 13 wherein:

(a) each source node is associated with a respective receive node and first direction control node, and each destination node is associated with a respective send node and second direction control node;

(b) a send switching arrangement is interposed between the send nodes and the alternate transmission paths;

(c) a receive switching arrangement is interposed between the alternate transmission paths and the receive nodes;

(d) a first direction control switching arrangement is interposed between the first direction control nodes and a control input of a number of tri-state drivers, each driver associated with a respective source node; and

(e) a second direction control switching arrangement is interposed between the second direction control nodes and a control input of a number of additional tri-state drivers, each additional tri-state driver associated with a respective send node.

18. (Previously Presented) A method for compensating for errors in a communications bus between a source node and a destination node, the bus including alternate transmission paths between the source and destination node on a common substrate, the method including the steps of:

(a) applying a test signal to a first one of the alternate transmission paths between the source node and the destination node;

(b) determining whether the test signal is properly received at the destination node; and

(c) if the test signal is not properly received at the destination node, switching to a second one of the alternate transmission paths between the source node and destination node.

19. (Original) The method of Claim 18 further including the steps of:

(a) applying a second test signal to the second one of the alternate transmission paths between the source node and the destination node; and

(b) determining whether the second test signal is properly received at the destination node.

20. (Original) The method of Claim 18 wherein the communications bus extends between a number of source nodes and a like number of destination nodes, and the bus includes a number of alternate transmission paths between each source node and a respective one of the destination nodes, and wherein the method further includes:

(a) applying a respective test signal to each alternate transmission path between each respective source node and its respective destination node;

(b) determining whether each respective test signal is properly received at the respective destination node; and

(c) for each respective test signal that is not properly received at the respective destination node, switching the respective source node to a different one of the alternate transmission paths between the respective source node and destination node.

21. (Original) The method of Claim 20 wherein the step of switching the respective source node to a different one of the alternate transmission paths between the respective source node and destination node includes applying a control signal to a switching device interposed between the source node and the alternate transmission paths associated with the respective source node.

22. (Original) The method of Claim 21 wherein each control signal is applied from a memory device associated with the communications bus.

23. (New) A communications bus connected between a source node and a destination node, the communications bus including:

(a) a number of alternate transmission paths extending between the source node and the destination node on a common substrate comprising a semiconductor chip;

(b) a source switching arrangement interposed between the source node and the alternate transmission paths, the source switching arrangement being operable to selectively connect the source node to a selected one of the alternate transmission paths and disconnect the source node from each other alternate transmission path;

(c) a destination switching arrangement interposed between the destination node and the alternate transmission paths, the destination switching arrangement being operable to selectively connect the destination node to the selected one of the alternate transmission paths and disconnect the destination node from each other alternate transmission path;

(d) test circuitry connected to the source node and destination node for applying a test signal to each alternate transmission path at initialization of the communication bus and for monitoring the destination node to determine whether the respective test signal is properly received at the destination node; and

(e) wherein a receive node and first direction control node are associated with the source node, and a send node and second direction control node are associated with the destination node;

(f) a send switching arrangement is interposed between the send node and each alternate transmission path;

(g) a receive switching arrangement is interposed between each alternate transmission path and the receive node;

(h) a first direction control switching arrangement is interposed between the first direction control node and a control input of a tri-state driver associated with the source node; and

(i) a second direction control switching arrangement is interposed between the second direction control node and a control input of a tri-state driver associated with the send node.

24. (New) The communication bus of claim 23 wherein the test circuitry is configured to apply the test signal once only.